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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,373	07/30/2003	Albert Birner	12816-095001	8955

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EXAMINER	
TRAN, THANH Y	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 09/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/630,373	BIRNER ET AL.	
	Examiner	Art Unit	
	Thanh Y. Tran	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-18 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7/30/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5 and 10-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Graimann et al (U.S. 6,207,494).

As to claim 1, Graimann et al discloses an apparatus and a corresponding method for fabricating a semiconductor trench structure (figures 2-4), the apparatus and a corresponding method comprising: providing a semiconductor substrate (gate 35); forming a trench (21) in the semiconductor substrate; filling the trench (21) with a filler material (37, 38); in a first thermal process having a first maximum temperature (900-1100°C) (see col. 11, lines 30-40, filling the trench at 900-1100°C), curing the filler material (37, 38), so that the filler material is thermally stable; removing the filler material (37) from an upper region of the trench (21) as far as a boundary surface to define a collar region (see Fig. 4); in a second thermal process having a second maximum temperature that is not significantly higher than the first maximum temperature, depositing a liner on the collar region and the boundary surface (see col. 6, lines 39-49, the second thermal process having a temperature of 900°C which is not significantly higher than the first maximum temperature (900-1100°C)); removing the liner (25) from the boundary surface (53), thereby exposing the filler material (38) (see Figs. 3-4); and removing the filler material (38) from a lower region of the trench (see Fig. 10).

As to claim 2, Graimann et al discloses an apparatus and a corresponding method for fabricating a semiconductor trench structure (figures 2-4), wherein filling the trench (21) with a filler material (37, 38) further comprises selecting a material from the group consisting of a liquid filler and a filler material ("polysilicon") that is able to flow (see col. 5, lines 34-47).

As to claim 3, Graimann et al discloses an apparatus and a corresponding method for fabricating a semiconductor trench structure (figures 2-4), further comprising selecting semiconductor trench structure (21) to be a trench capacitor (32) (see col. 4, lines 35-37).

As to claim 4, Graimann et al discloses an apparatus and a corresponding method for fabricating a semiconductor trench structure (figures 2-4), further comprising: in a third thermal process having a third maximum temperature, providing a second liner (22) on the trench wall prior to filling the trench (21) (see col. 6, lines 50-61), removing the second liner (22) from the lower region of the trench (21) (see Fig. 10A), and using the first liner (25) as a mask after removal of the filler material (37) (see Figs. 3-4).

As to claim 5, Graimann et al discloses an apparatus and a corresponding method for fabricating a semiconductor trench structure (figures 2-4), further comprising selecting the second thermal process (see col. 6, lines 39-49, the second thermal process having a temperature of 900°C) to be a chemical vapor deposition process (see col. 6, line 62 - col. 7, line 7).

As to claim 10, Graimann et al discloses an apparatus and a corresponding method for fabricating a semiconductor trench structure (figures 2-4), comprising: applying the filler material (37, 38) using a deposition process and causing the filler material to flow (see col. 6, line 62 - col. 7, line 7).

As to claim 11, Graimann et al discloses an apparatus and a corresponding method for fabricating a semiconductor trench structure (figures 2-4), the process further comprising: baking the structure to cause the filler material to flow, and curing the filler material (37, 38) (see col. 11, lines 30-40, filling the trench at 900-1100°C).

As to claims 12 and 13, Graimann et al discloses an apparatus and a corresponding method for fabricating a semiconductor trench structure (figures 2-4), further comprising: removing the filler material by an incineration process ("plasma etching technique"); selecting the incineration process to be an oxygen plasma process ("plasma etching technique") (see col. 7, lines 8-29; and col. 8, line 65 – col. 9, line 29).

As to claim 14, Graimann et al discloses an apparatus and a corresponding method for fabricating a semiconductor trench structure (figures 2-4), further comprising: applying a bonding agent to a surface of the trench ("tapered trench") prior to filling the trench (see col. 10, lines 38-60; and col. 7, lines 7-29).

As to claim 15, Graimann et al discloses an apparatus and a corresponding method for fabricating a semiconductor trench structure (figures 2-4), comprising: conditioning a surface of the trench prior to filling the trench (21) (see col. 7, lines 7-29).

As to claim 16, Graimann et al discloses an apparatus and a corresponding method for fabricating a semiconductor trench structure (figures 2-4), further comprising: using a plasma process ("plasma etching technique") for conditioning the surface of the trench (see col. 7, lines 8-29; and col. 8, line 65 – col. 9, line 29).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Graimann et al (U.S. 6,207,494).

As to claims 6 and 8, Graimann et al does not disclose an apparatus and a corresponding method comprising: selecting the first maximum temperature to be at most 500°C; selecting the filler material to be an organic polymer that is thermally stable between 400°C and 500°C. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Graimann et al by using a first maximum temperature to be at most 500°C, and the temperature between 400°C and 500°C for selecting the filler material for producing undoped polysilicon material at the bottom of the trench and preventing degrading any temperature-sensitive layers deposited in earlier processing steps, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Graimann et al (U.S. 6,207,494) in view of Lu et al (U.S. 6,680,249).

As to claim 7, Graimann et al does not disclose an apparatus and a corresponding method comprising: selecting the third thermal process to be a conformal deposition process. Lu et al (U.S. 6,680,249) discloses in figures 3C-3E an apparatus a corresponding method comprising a

conformal deposition process. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus and corresponding method of Graimann et al by using a conformal deposition process as taught by Lu et al for the purpose of providing a sufficient barrier on the sidewalls of the trench (see col. 3, lines 40-54 in Lu et al).

6. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Graimann et al (U.S. 6,207,494) in view of Yu et al (U.S. 6,025,272).

As to claim 9, Graimann et al does not disclose an apparatus and a corresponding method comprising: applying the filler material using a spin-on process. Yu et al (U.S. 6,025,272) discloses an apparatus and a corresponding method comprising: applying the filler material using a spin-on process (see col. 6, lines 20-30). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus and a corresponding method of Graimann et al by using a spin-on process for filling the material as taught by Yu for the purpose of causing the surface of the spin-on material to be relatively smooth (see col. 6, lines 20-30 in Yu).

7. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Graimann et al (U.S. 6,207,494) in view of Yoo et al (U.S. 2002/0197823).

As to claims 17 and 18, Graimann et al does not disclose an apparatus and a corresponding method comprising: selecting the liner to be an Al_2O_3 liner; applying the Al_2O_3 liner at temperature between 200°C and 300°C. Yoo et al discloses in figures 6, 7 and 8 an apparatus and a corresponding method comprising: selecting the liner (109) to be an Al_2O_3 liner;

and applying the Al_2O_3 material for a liner (109) (see col. 2, line 37-50; and col. 6, line 60 – col. 7, line 7). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus and a corresponding method of Graimann et al by using Al_2O_3 material for a liner as taught by Yoo et al for protecting the trench due to high density and providing an easy etching process (see col. 2, lines 37-50 in Yoo et al). It also would have been obvious to modify the apparatus and corresponding method of Graimann by applying a temperature between 200°C and 300°C for the liner for preventing degrading any temperature-sensitive layers deposited in earlier processing steps, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Halle et al (U.S. 5,877,061) discloses Methods for roughening and volume expansion of trench sidewalls to form high capacitance trench cell for high density dram applications.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TYT

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